Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) An addressing mechanism, comprising:

a first set of parallel[[,]] co-planar conductive control lines, wherein each control line of said first set of conductive control lines has an adjustable in-line impedance configured to exhibit either a low in-line impedance state or a high in-line impedance state;

a second set of parallel[[,]] co-planar conductive control lines, wherein said second set of conductive control lines are spaced apart in relation to said first set of conductive control lines, wherein a plane of said second set of conductive control lines is parallel to a plane of said first set of conductive control lines, wherein control lines of said second set of conductive control lines ~~are perpendicular to~~ cross over the control lines of said first set of conductive control lines thereby forming a plurality of crossover regions in an inactivated state, wherein each of the plurality of crossover regions is operable to be actuated to an activated state;

a first select mechanism configured to selectively ~~apply an~~ adjust the in-line impedance ~~to~~ of a selected control line of said first set of conductive control lines from the high in-line impedance to the low in-line impedance state for a duration of a time cycle;

a first voltage signal source configured to simultaneously apply a first drive voltage to all control lines of said first set of conductive control lines to electrically charge said first set of conductive control lines; and

a second select mechanism configured to selectively apply (1) a second drive voltage to ~~each conductive line~~ zero or more control lines of said second set of conductive control lines to electrically charge said zero or more control lines, and (2) a third drive voltage to the remaining control lines of said second set of conductive control lines to electrically discharge said remaining control lines,

wherein prior to the time cycle (1) all control lines of said first set of conductive control lines exhibit the high in-line impedance state, (2) the first drive voltage is simultaneously applied to all control lines of said first set of conductive control lines, (3) the second drive voltage is applied to the zero or more control lines of said second set of conductive control lines, and (4) the third drive voltage is applied to the remaining control lines of said second set of conductive control lines.

2. (Currently amended) The addressing mechanism as recited in claim 1, wherein said first select mechanism is further configured to selectively toggle each control ~~lines~~ line of said first set of conductive control lines between ~~a low~~ the high in-line impedance state and ~~a high~~ the low in-line impedance state.

3. (Currently amended) The addressing mechanism as recited in claim 2, wherein said first ~~selected~~ select mechanism further comprises:

a row select sequencer configured to select the selected control line and initiate the time cycle ~~sequentially activate subsequent control lines in said first set of conductive control lines, wherein a selected control line in said first set of conductive control lines is placed in a low impedance state while non-selected control lines in said first set of conductive control lines are placed in a high impedance state~~;

a clock mechanism configured to determine [[a]] the duration of the time cycle wherein ~~said selected~~ the ~~single~~ selected control line is in said low in-line impedance state; and

a synchronizing mechanism configured to ~~synchronize loading and encoding of~~ parallel load data to ~~said clocking mechanism and said selected control line such that said data is loaded and processed during said duration of time said selected control line is in said low impedance state~~ each control line of said second set of conductive control lines prior to the time cycle.

4. (Currently amended) The addressing mechanism as recited in claim 1, wherein ~~a region of overlap between a conductive line of said first set of conductive control lines and a conductive line of said second set of conductive control lines is selectively charged and discharged~~ for the

duration of the time cycle the first select mechanism adjusts the impedance of the selected control line to the low in-line impedance state thereby making the selected control line addressable, and wherein during the time cycle each of the plurality of crossover regions formed by the low in-line impedance selected control line and said zero or more control lines of said second set of conductive control lines actuates to the activated state by electrically charging each of said crossover regions so as to exceed an activation threshold, wherein during the time cycle each of the plurality of crossover regions formed by the low in-line impedance selected control line and said remaining control lines of said second set of conductive control lines discharges to the inactivated state by electrically discharging each of said crossover regions below a deactivation threshold.

5. (Currently amended) The addressing mechanism as recited in claim 4, wherein ~~a cycle time for selectively charging and discharging said region of overlap is sufficiently short such that an active device will not be deactivated and an inactive device will not be activated, wherein said cycle time for selectively charging and discharging said region of overlap is sufficiently long such that an active device will discharge to below an activation threshold and an inactive device will charge beyond said activation threshold~~ the time cycle is not long enough to sufficiently charge or discharge any one of the remaining plurality of crossover regions formed by the high in-line impedance remaining control lines of said first set of conductive control lines and each control line of said second set of conductive control lines past the activation threshold to switch from the inactivated state to the activated state or past the deactivation threshold to switch from the activated state to the inactivated state.

6. (Currently amended) The addressing mechanism as recited in claim 1, wherein control lines in said second set of conductive control lines are equally split into two collinear[[,]] coplanar halves with sufficient physical separation to ensure electrical isolation between ~~them~~ the two halves thereby forming a first half set and a second half set, wherein the control lines in said first set of conductive control lines are equally divided between the first half set and the second half set.

7. (Currently amended) The addressing mechanism [[sad]] as recited in claim 1, wherein a polarity of a field generated between control lines of said first set of conductive control lines and control lines of said second set of conductive controls lines are reversed in a cyclic manner.

8. (Original) The addressing mechanism as recited in claim 7, wherein said polarity of said field is reversed in said cyclic manner by driving a pair of comparators from a voltage divider and oscillating a control logic signal distributed across appropriate reference potentials of opposing polarity.

9. (Currently amended) The addressing mechanism as recited in claim 1, wherein each control line of said first set of ~~parallel, co-planar~~ conductive control lines is driven at both ends from the first voltage signal source, and wherein each of the zero or more control lines of said second set of ~~parallel, co-planar~~ conductive control lines ~~are~~ is driven at both ends from a second voltage ~~common~~ signal source, and wherein each of the remaining control lines of said second set of conductive control lines is driven at both ends from a third voltage signal source.

10. (Currently amended) The addressing mechanism as recited in claim [[9]] 6, wherein [[a]] the first drive ~~set of~~ voltage ~~levels are~~ is applied to all control lines of said first set of ~~parallel, co-planar~~ conductive control lines, wherein [[a]] the second select mechanism applies the second ~~set of~~ drive voltage ~~levels are applied to said second set of parallel, co-planar conductive control lines wherein an activated device at a region of overlap between a conductive line of said first set of conductive control lines and a conductive line of said second set of conductive control lines is deactivated when a difference between one of said second set of voltage levels and one of said first set of voltage levels is below a first threshold, wherein an activated device at said region of overlap is deactivated when a difference between one of said second set of voltage levels and one of said first set of voltage levels is less than a first threshold, wherein a deactivated device at said region of overlap is activated when a difference between one of said second set of voltage levels and one of said first set of voltage levels exceeds a second threshold~~ to zero or more control lines in said first half set and the third drive voltage to the remaining control lines in said first half set, and wherein the second select mechanism concurrently applies the second drive voltage to zero

or more control lines in said second half set and the third drive voltage to the remaining control lines in said second half set, and wherein the first select mechanism adjusts the in-line impedance of both a first selected control line in said first half set and a second selected control line in said second half set to the low in-line impedance state for the duration of the time cycle.

11. (Currently amended) The addressing mechanism as recited in claim 1, wherein each ~~conductive~~ control line of said first set of ~~parallel, co-planar~~ conductive control lines comprises a material configured to selectively change its resistance across the entire ~~conductive~~ control line.

12. (Currently amended) The addressing mechanism as recited in claim 11, wherein said material of said first set of ~~parallel, co-planar~~ conductive control lines changes its resistance upon application of an appropriate ~~potential~~ voltage difference between a first and a second conductive line spatially disposed on opposite sides of each ~~conductive~~ control line of said first set of ~~parallel, co-planar~~ conductive control lines.

13. (Original) The addressing mechanism as recited in claim 12, wherein said material comprises doped perovskites.

14. (Currently amended) A display, comprising:

a first set of parallel[[,]] co-planar conductive control lines, wherein each control line of said first set of conductive control lines has an adjustable in-line impedance configured to exhibit either a low in-line impedance state or a high in-line impedance state;

a second set of parallel[[,]] co-planar conductive control lines, wherein said second set of conductive control lines are spaced apart in relation to said first set of conductive control lines, wherein a plane of said second set of conductive control lines is parallel to a plane of said first set of conductive control lines, wherein control lines of said second set of conductive control lines ~~are perpendicular to~~ cross over the control lines of said first set of conductive control lines thereby forming a plurality of crossover regions in an inactivated state, wherein each of the plurality of crossover regions is operable to be actuated to an activated state;

a matrix of pixels overlapping between said first set of parallel[[,]] co-planar conductive control lines and said second set of parallel[[,]] co-planar conductive control lines;

a first select mechanism coupled to said matrix of pixels, wherein said first select mechanism is configured to selectively ~~apply an~~ adjust the in-line impedance ~~to~~ of a selected control line of said first set of conductive control lines from the high in-line impedance state to the low in-line impedance state for a duration of a time cycle;

a first voltage signal source configured to simultaneously apply a first drive voltage to all control lines of said first set of conductive control lines to electrically charge said first set of conductive control lines; and

a second select mechanism coupled to said matrix of pixels, wherein said second select mechanism is configured to selectively apply (1) a second drive voltage to ~~each conductive line~~ zero or more control lines of said second set of conductive control lines to electrically charge said zero or more control lines, and (2) a third drive voltage to the remaining control lines of said second set of conductive control lines to electrically discharge said remaining control lines,

wherein prior to the time cycle (1) all control lines of said first set of conductive control lines exhibit the high in-line impedance state, (2) the first drive voltage is simultaneously applied to all control lines of said first set of conductive control lines, (3) the second drive voltage is applied to the zero or more control lines of said second set of conductive control lines, and (4) the third drive voltage is applied to the remaining control lines of said second set of conductive control lines.

15. (Currently amended) The display as recited in claim 14, wherein said first select mechanism is further configured to selectively toggle each control ~~lines~~ line of said first set of conductive control lines between ~~a low~~ the high in-line impedance state and ~~a high~~ the low in-line impedance state.

16. (Currently amended) The display as recited in claim 15, wherein said first ~~selected~~ select mechanism further comprises:

a row select sequencer configured to select the selected control line and initiate the time cycle ~~sequentially activate subsequent control lines in said first set of conductive control lines, wherein a selected control line in said first set of conductive control lines is placed in a low impedance state while non-selected control lines in said first set of conductive control lines are placed in a high impedance state~~;

a clock mechanism configured to determine [[a]] the duration of the time cycle wherein the ~~said~~ selected control line is in said low in-line impedance state; and

a synchronizing mechanism configured to ~~synchronize loading and encoding of~~ parallel load data to ~~said clocking mechanism and said selected control line such that said data is loaded and processed during said duration of time said selected control line is in said low impedance state~~ each control line of said second set of conductive control lines prior to the time cycle.

17. (Currently amended) The display as recited in claim 14, wherein ~~a pixel of said matrix of pixels between a conductive line of said first set of conductive control lines and a conductive line of said second set of conductive control lines is selectively charged and discharged~~ for the duration of the time cycle the first select mechanism adjusts the impedance of the selected control line to the low in-line impedance state thereby making the selected control line addressable, and wherein during the time cycle each of the plurality of crossover regions formed by the low in-line impedance selected control line and said zero or more control lines of said second set of conductive control lines actuates to the activated state by electrically charging each of said crossover regions so as to exceed an activation threshold, wherein during the time cycle each of the plurality of crossover regions formed by the low in-line impedance selected control line and said remaining control lines of said second set of conductive control lines discharges to the inactivated state by electrically discharging each of said crossover regions below a deactivation threshold.

18. (Currently amended) The display as recited in claim 17, wherein ~~a cycle time for selectively charging and discharging said pixel of said matrix of pixels is sufficiently short such that an active device will not be deactivated and an inactive device will not be activated, wherein said cycle time for selectively charging and discharging said pixel of said matrix of pixels is~~

~~sufficiently long such that an active device will discharge to below an activation threshold and an inactive device will charge beyond said activation threshold~~ the time cycle is not long enough to sufficiently charge or discharge any one of the remaining plurality of crossover regions formed by the high in-line impedance remaining control lines of said first set of conductive control lines and each control line of said second set of conductive control lines past the activation threshold to switch from the inactivated state to the activated state or past the deactivation threshold to switch from the activated state to the inactivated state.

19. (Currently amended) The display as recited in claim 14, wherein control lines in said second set of conductive control lines are equally split into two collinear[[,]] coplanar halves with sufficient physical separation to ensure electrical isolation between ~~them~~ the two halves thereby forming a first half set and a second half set, wherein the control lines in said first set of conductive control lines are equally divided between the first half set and the second half set.

20. (Original) The display as recited in claim 14, wherein a polarity of a field generated between control lines of said first set of conductive control lines and control lines of said second set of conductive controls lines are reversed in a cyclic manner.

21. (Original) The display as recited in claim 20, wherein said polarity of said field is reversed in said cyclic manner by driving a pair of comparators from a voltage divider and oscillating a control logic signal distributed across appropriate reference potentials of opposing polarity.

22. (Currently amended) The display as recited in claim 14, wherein each control line of said first set of ~~parallel, co-planar~~ conductive control lines is driven at both ends from the first voltage signal source, and wherein each of the zero or more control lines of said second set of ~~parallel, co-planar~~ conductive control lines ~~are~~ is driven at both ends from a second voltage ~~common~~ signal source, and wherein each of the remaining control lines of said second set of conductive control lines is driven at both ends from a third voltage signal source.

23. (Currently amended) The display as recited in claim [[22]] 19, wherein [[a]] the first drive ~~set of~~ voltage ~~levels are~~ is applied to all control lines of said first set of ~~parallel, co-planar~~ conductive control lines, wherein [[a]] the second select mechanism applies the second ~~set of~~ drive voltage ~~levels are applied to said second set of parallel, co-planar conductive control lines, wherein an activated device at a pixel of said matrix of pixels between a conductive line of said first set of conductive control lines and a conductive line of said second set of conductive control lines is deactivated when a difference between one of said second set of voltage levels and one of said first set of voltage levels is below a first threshold, wherein an activated device at said pixel of said matrix of pixels is deactivated when a difference between one of said second set of voltage levels and one of said first set of voltage levels is less than a first threshold, wherein a deactivated device at said pixel of said matrix of pixels is activated when a difference between one of said second set of voltage levels and one of said first set of voltage levels exceeds a second threshold~~ to zero or more control lines in said first half set and the third drive voltage to the remaining control lines in said first half set, and wherein the second select mechanism concurrently applies the second drive voltage to zero or more control lines in said second half set and the third drive voltage to the remaining control lines in said second half set, and wherein the first select mechanism adjusts the in-line impedance of both a first selected control line in said first half set and a second selected control line in said second half set to the low in-line impedance state for the duration of the time cycle.

24. (Currently amended) The display as recited in claim 14, wherein each ~~conductive~~ control line of said first set of ~~parallel, co-planar~~ conductive control lines comprises a material configured to selectively change its resistance across the entire ~~conductive~~ control line.

25. (Currently amended) The display as recited in claim 24, wherein said material of said first set of ~~parallel, co-planar~~ conductive control lines changes its resistance upon application of an appropriate ~~potential~~ voltage difference between a first and a second conductive line spatially disposed on opposite sides of each ~~conductive~~ control line of said first set of ~~parallel, co-planar~~ conductive control lines.

26. (Original) The display as recited in claim 25, wherein said material comprises doped perovskites.

27. (Currently amended) A system, comprising:

a processor;

a memory unit;

an input mechanism;

a display; and

a bus system for coupling the processor to the memory unit, input mechanism and display,[[;]]

wherein said display comprises:

a first set of parallel[[,]] co-planar conductive control lines, wherein each control line of said first set of conductive control lines has an adjustable in-line impedance configured to exhibit either a low in-line impedance state or a high in-line impedance state;

a second set of parallel[[,]] co-planar conductive control lines, wherein said second set of conductive control lines are spaced apart in relation to said first set of conductive control lines, wherein a plane of said second set of conductive control lines is parallel to a plane of said first set of conductive control lines, wherein control lines of said second set of conductive control lines ~~are perpendicular to~~ cross over the control lines of said first set of conductive control lines thereby forming a plurality of crossover regions in an inactivated state, wherein each of the plurality of crossover regions is operable to be actuated to an activated state;

a matrix of pixels overlapping between said first set of parallel[[,]] co-planar conductive control lines and said second set of parallel[[,]] co-planar conductive control lines;

a first select mechanism coupled to said matrix of pixels, wherein said first select mechanism is configured to selectively ~~apply an~~ adjust the in-line impedance ~~to~~ of a selected control line of said first set of conductive control lines from the high in-line impedance state to the low in-line impedance state for a duration of a time cycle;

a first voltage signal source configured to simultaneously apply a first drive voltage to all control lines of said first set of conductive control lines to electrically charge said first set of conductive control lines; and

a second select mechanism coupled to said matrix of pixels, wherein said second select mechanism is configured to selectively apply (1) a second drive voltage to ~~each conductive line~~ zero or more control lines of said second set of conductive control lines to electrically charge said zero or more control lines, and (2) a third drive voltage to the remaining control lines of said second set of conductive control lines to electrically discharge said remaining control lines,

wherein prior to the time cycle (1) all control lines of said first set of conductive control lines exhibit the high in-line impedance state, (2) the first drive voltage is simultaneously applied to all control lines of said first set of conductive control lines, (3) the second drive voltage is applied to the zero or more control lines of said second set of conductive control lines, and (4) the third drive voltage is applied to the remaining control lines of said second set of conductive control lines.

28. (Currently amended) The system as recited in claim 27, wherein said first select mechanism is further configured to selectively toggle each control ~~lines~~ line of said first set of conductive control lines between ~~a low~~ the high in-line impedance state and ~~a high~~ the low in-line impedance state.

29. (Currently amended) The system as recited in claim 28, wherein said first ~~selected~~ select mechanism further comprises:

a row select sequencer configured to select the selected control line and initiate the time cycle ~~sequentially activate subsequent control lines in said first set of conductive control lines, wherein a selected control line in said first set of conductive control lines is placed in a low impedance state while non-selected control lines in said first set of conductive control lines are placed in a high impedance state~~;

a clock mechanism configured to determine [[a]] the duration of the time cycle wherein the ~~said~~ selected control line is in said low in-line impedance state; and

a synchronizing mechanism configured to ~~synchronize loading and encoding of~~ parallel load data to ~~said clocking mechanism and said selected control line such that said data is loaded~~

~~and processed during said duration of time said selected control line is in said low impedance state~~ each control line of said second set of conductive control lines prior to the time cycle.

30. (Currently amended) The system as recited in claim 27, wherein ~~a pixel of said matrix of pixels between a conductive line of said first set of conductive control lines and a conductive line of said second set of conductive control lines is selectively charged and discharged~~ for the duration of the time cycle the first select mechanism adjusts the impedance of the selected control line to the low in-line impedance state thereby making the selected control line addressable, and wherein during the time cycle each of the plurality of crossover regions formed by the low in-line impedance selected control line and said zero or more control lines of said second set of conductive control lines actuates to the activated state by electrically charging each of said crossover regions so as to exceed an activation threshold, wherein during the time cycle each of the plurality of crossover regions formed by the low in-line impedance selected control line and said remaining control lines of said second set of conductive control lines discharges to the inactivated state by electrically discharging each of said crossover regions below a deactivation threshold.

31. (Currently amended) The system as recited in claim 30, wherein ~~a cycle time for selectively charging and discharging said pixel of said matrix of pixels is sufficiently short such that an active device will not be deactivated and an inactive device will not be activated, wherein said cycle time for selectively charging and discharging said pixel of said matrix of pixels is sufficiently long such that an active device will discharge to below an activation threshold and an inactive device will charge beyond said activation threshold~~ the time cycle is not long enough to sufficiently charge or discharge any one of the remaining plurality of crossover regions formed by the high in-line impedance remaining control lines of said first set of conductive control lines and each control line of said second set of conductive control lines past the activation threshold to switch from the inactivated state to the activated state or past the deactivation threshold to switch from the activated state to the inactivated state.

32. (Currently amended) The system as recited in claim 27, wherein control lines in said second set of conductive control lines are equally split into two collinear[[,]] coplanar halves with sufficient physical separation to ensure electrical isolation between ~~them~~ the two halves thereby forming a first half set and a second half set, wherein the control lines in said first set of conductive control lines are equally divided between the first half set and the second half set.

33. (Original) The system as recited in claim 27, wherein a polarity of a field generated between control lines of said first set of conductive control lines and control lines of said second set of conductive controls lines are reversed in a cyclic manner.

34. (Original) The system as recited in claim 33, wherein said polarity of said field is reversed in said cyclic manner by driving a pair of comparators from a voltage divider and oscillating a control logic signal distributed across appropriate reference potentials of opposing polarity.

35. (Currently amended) The system as recited in claim 27, wherein each control line of said first set of ~~parallel, co-planar~~ conductive control lines is driven at both ends from the first voltage signal source, and wherein each of the zero or more control lines of said second set of ~~parallel, co-planar~~ conductive control lines ~~are~~ is driven at both ends from a second voltage ~~common~~ signal source, and wherein each of the remaining control lines of said second set of conductive control lines is driven at both ends from a third voltage signal source.

36. (Currently amended) The system as recited in claim [[35]] 32, wherein [[a]] the first drive ~~set of~~ voltage ~~levels are~~ is applied to all control lines of said first set of ~~parallel, co-planar~~ conductive control lines, wherein [[a]] the second select mechanism applies the second ~~set of~~ drive voltage ~~levels are applied to said second set of parallel, co-planar conductive control lines, wherein an activated device at a pixel of said matrix of pixels between a conductive line of said first set of conductive control lines and a conductive line of said second set of conductive control lines is deactivated when a difference between one of said second set of voltage levels and one of said first set of voltage levels is below a first threshold, wherein an activated device at said pixel~~

~~of said matrix of pixels is deactivated when a difference between one of said second set of voltage levels and one of said first set of voltage levels is less than a first threshold, wherein a deactivated device at said pixel of said matrix of pixels is activated when a difference between one of said second set of voltage levels and one of said first set of voltage levels exceeds a second threshold~~ to zero or more control lines in said first half set and the third drive voltage to the remaining control lines in said first half set, and wherein the second select mechanism concurrently applies the second drive voltage to zero or more control lines in said second half set and the third drive voltage to the remaining control lines in said second half set, and wherein the first select mechanism adjusts the in-line impedance of both a first selected control line in said first half set and a second selected control line in said second half set to the low in-line impedance state for the duration of the time cycle.

37. (Currently amended) The system as recited in claim 27, wherein each ~~conductive~~ control line of said first set of ~~parallel, co-planar~~ conductive control lines comprises a material configured to selectively change its resistance across the entire ~~conductive~~ control line.

38. (Currently amended) The system as recited in claim 37, wherein said material of said first set of ~~parallel, co-planar~~ conductive control lines changes its resistance upon application of an appropriate ~~potential~~ voltage difference between a first and a second conductive line spatially disposed on opposite sides of each ~~conductive~~ control line of said first set of ~~parallel, co-planar~~ conductive control lines.

39. (Original) The system as recited in claim 38, wherein said material comprises doped perovskites.

40. (new) The addressing mechanism as recited in claim 1, wherein each of the plurality of crossover regions is operable to be actuated to the activated state by applying a sufficient electrical charge to create a voltage difference across said first and second conductive control lines in the crossover region so as to cause local movement of one control line of said first and

second conductive control lines towards the other control line of said first and second conductive control lines.

41. (new) The addressing mechanism as recited in claim 14, wherein each of the plurality of crossover regions is operable to be actuated to the activated state by applying a sufficient electrical charge to create a voltage difference across said first and second conductive control lines in the crossover region so as to cause local movement of one control line of said first and second conductive control lines towards the other control line of said first and second conductive control lines.